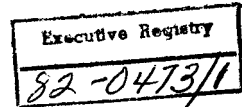DIRECTOR OF CENTRAL INTELLIGENCE

*Science and Technology Advisory Panel*

1 March 1982

MEMORANDUM FOR:   Deputy Director of Central Intelligence

SUBJECT:          Technology Transfer

    1.   I share many of the concerns you voiced in your AAAS speech of last month.  But it is not only the academic community that should be admonished. The enclosed VHSIC Notes is an excellent example of the open publication of technical information by the Defense Department.  While the VHSIC contracts are unclassified, I believe the publication in the Notes of the detailed progress in this technology, the status of various programs and planned activities, all presented in detail, provides a penetrating view of where we stand in this critical technology.

    2.   I also wish to call your attention to a book just published by J. Wiley:

    VHSIC (Very High Speed Integrated Circuits) Technologies and Tradeoffs by Arpod Barns.  I believe it is based on DoD-sponsored research but have not been able to get a copy.  The local bookstores report that it has been a best seller over the last three weeks.  I note that Washington is not Silicon Valley.
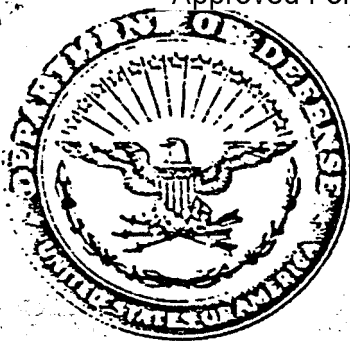
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# VERY HIGH SPEED INTEGRATED CIRCUITS PROGRAM

# VHSIC NOTES

## EDITORIAL: VHSIC PROGRESS

Larry W. Sumney, OUSDRE
VHSIC Program Director

The VHSIC Program is progressing well and continues to attract widespread attention as a model for other program areas in the DoD technology base. In particular, the management structure is maturing as a cohesive entity with effective support from the three Services. Currently, program management is focusing attention on the several aspects of the program discussed below in order to assure continued progress toward the defined goals.

Design validation procedures for VHSIC chips are required at all complexity levels and are not now being addressed in sufficient depth by the Phase I contractors. Also, the various models and model parameters used in the validation procedures do not seem to be adequate in many cases. Consideration is being given to the organization of a workshop to address these issues as well as program support to a standard hardware descriptive language.

On-chip testing and fault-tolerant designs also do not appear to be receiving the attention required, although they are an important contractual requirement. Approaches being followed appear to emphasize "stuck-at" faults and non-concurrent testing which may address design and manufacturing errors adequately but not important operational testing requirements. This area will be reviewed carefully as chip designs mature.

The technology insertion efforts of the Phase I prime contractors vary considerably. In some instances, the additional chip designs resulting from the expanded number of applications could over-extend the capabilities of the available staff with a resulting degraded performance. In others, a very conservative approach has been adopted, limiting potential applications. DoD project offices have shown less initiative in VHSIC technology insertion to date but this is expected to change as a result of current information dissemination activities. Overall, this area has received considerable attention during the past several months and much progress has been made.

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